

FIG. -1A

Title: MIXED SIGNAL SYNTHESIS
 Inventors: Michael J. Demler
 Application No.: 09/589,966
 Filing Date: June 8, 2000
 Docket No.: CADE-01016US0
 Attorney: Karl F. Kenna

Art Unit: 2128
 Telephone No. (415) 362-3800

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Antrim's Synthesis Methodology

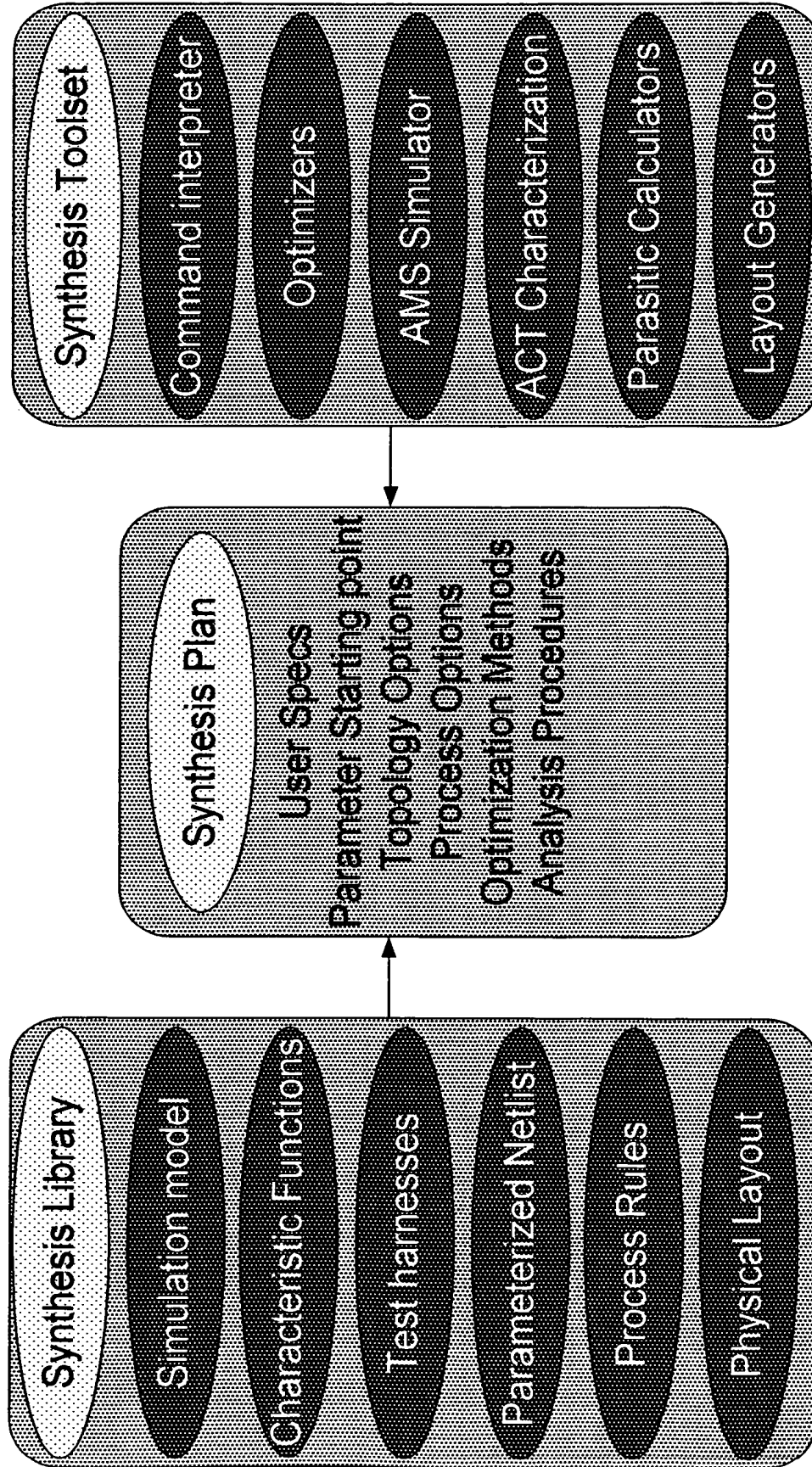
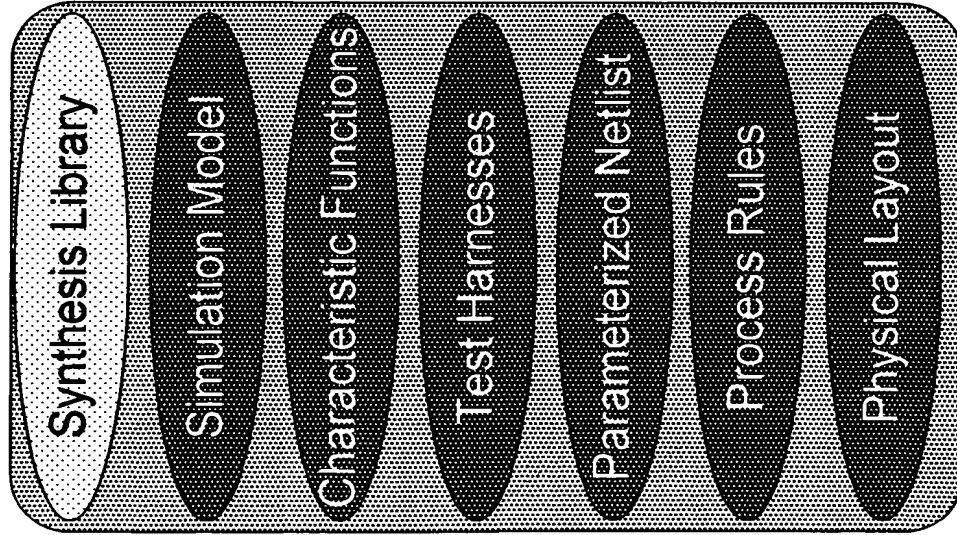


FIG. - 1B

Major Components of Antrin-MSS

Synthesis Library

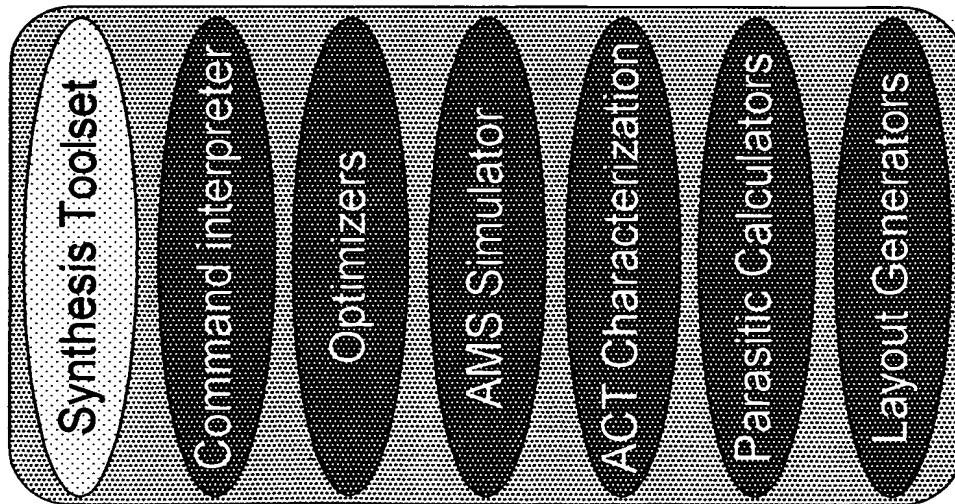


- Simulation models in Verilog-AMS
 - represent library functions , parameterized to user's performance specifications
- Characteristic functions of design parameters
 - model circuit performance behavior during optimization
- Test harnesses and characterization plans
 - developed with Antrim-ACT
- Netlists of mixed-signal functions
 - working circuits, parameterized for sizing to achieve user's performance specifications
- Process technology files - models and design rules
- Synthesizable layout cells

FIG. -1C

Major Components of Antrim-MSS

Synthesis Toolset



- Antrim-MSS Command Interpreter
 - extensions to Perl scripting language for synthesis plan execution
- Optimizers
 - toolkit of algorithms for sizing of design parameters
- Antrim-AMS
 - for simulation of characteristic functions, behavioral models and sized netlist
- Antrim-ACT
 - for development of characteristic functions, analytical models, test harnesses, circuit characterization
- Parasitic calculators
 - layout parasitic estimation from process rules and sized netlist
- Layout generators

FIG. - 1D

Major Components of Antrim-MSS

Synthesis Plans

- Blueprints for the successful synthesis of mixed-signal IP
- Developed by expert mixed-signal IC designers using MSS and ACT plan development tools
- Programmed series of steps for circuit partitioning, model selection, sizing and optimization
- Specifications of design parameters to be used as optimization variables
- Specifications of performance characteristics to be used as optimization goals
- Steps for process retargeting
- Antrim-ACT characterization plan
 - Experiments
 - Test harnesses
 - Stimuli and other controls

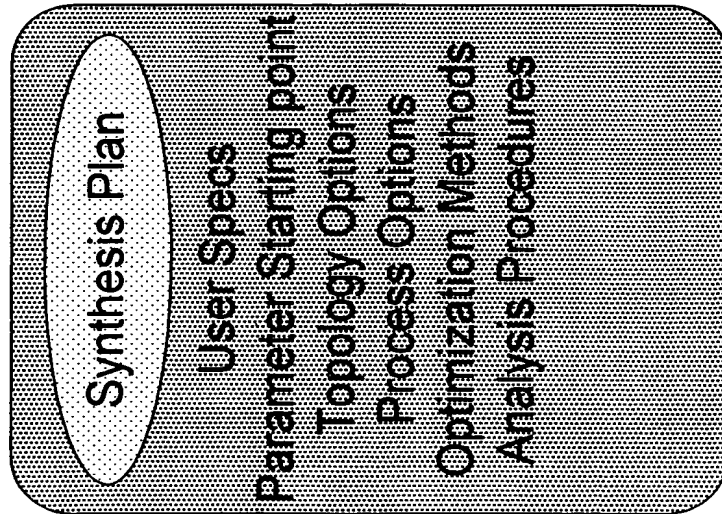


FIG. - 1E

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Plan Author Design Flow

- Design Partitioning
- Characterization
- Model Development
 - circuit
 - behavioral
 - analytic
- Setup Performance Parameters
 - measurements
 - test harnesses
- Set Design Parameters
- Define Optimization Steps

FIG. - 1F

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Plan User Design Flow

- Select Function
- Specify Process
- Performance Specification
- Execute Plan
- Verification of Results

FIG. - 1G

Antrim-MSS Architecture

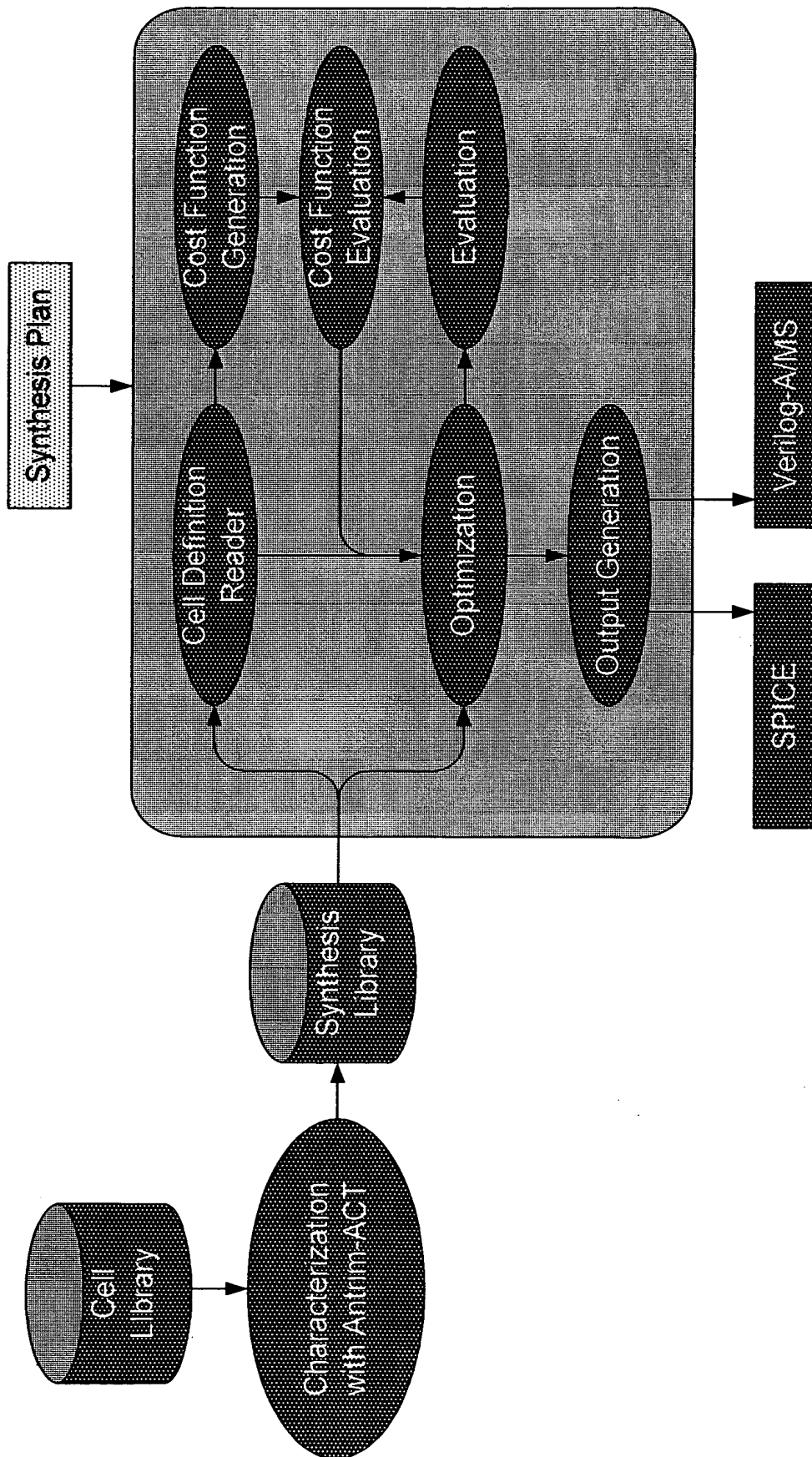


FIG. - 2

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Development of a Synthesizable VCO

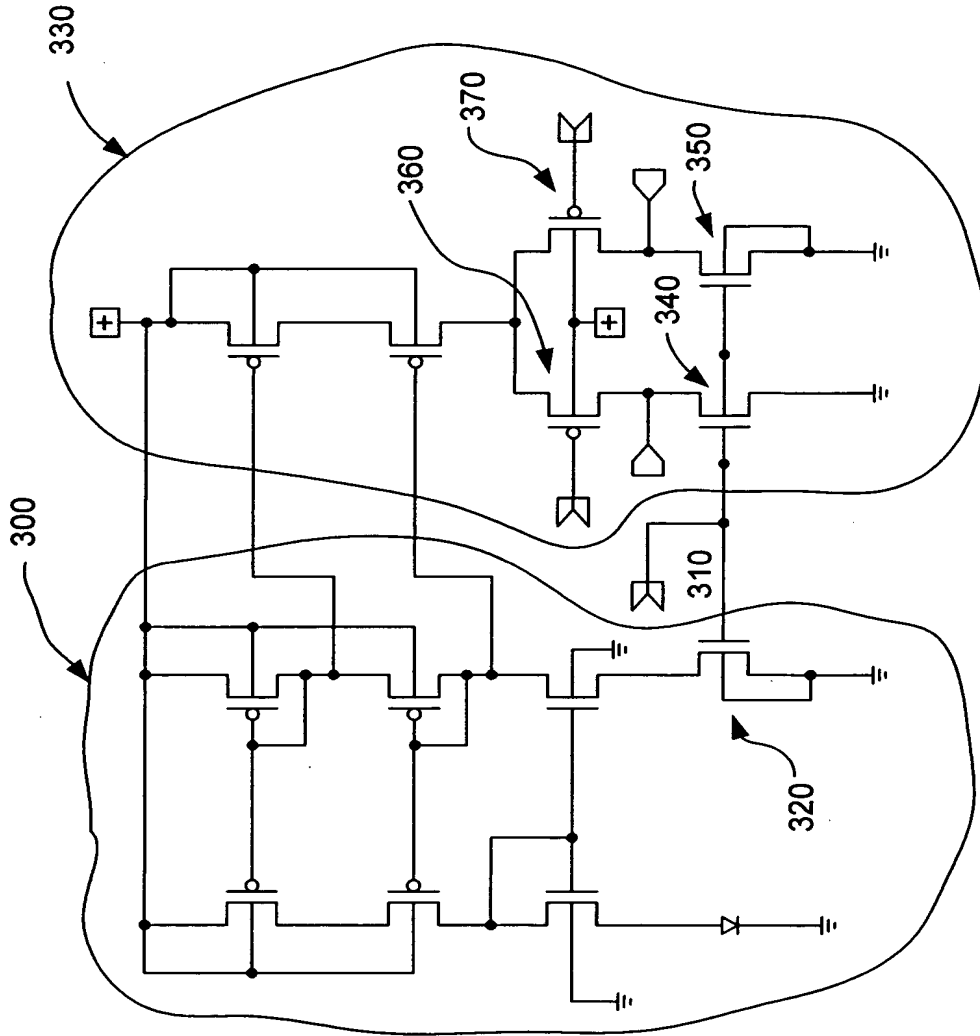


FIG. - 3

- Circuit features:
 - Three cells: bias generator, differential delay cell, level restore
 - Eight delay stages for 100 MHz - 200 MHz operation
- Performance parameters:
 - power
 - center frequency
- Optimization plan:
 - size delay cell and bias circuit to achieve user's specifications

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Cost Function

- User-specified performance specs are formulated into a single cost function
- Optimization seeks a zero cost solution

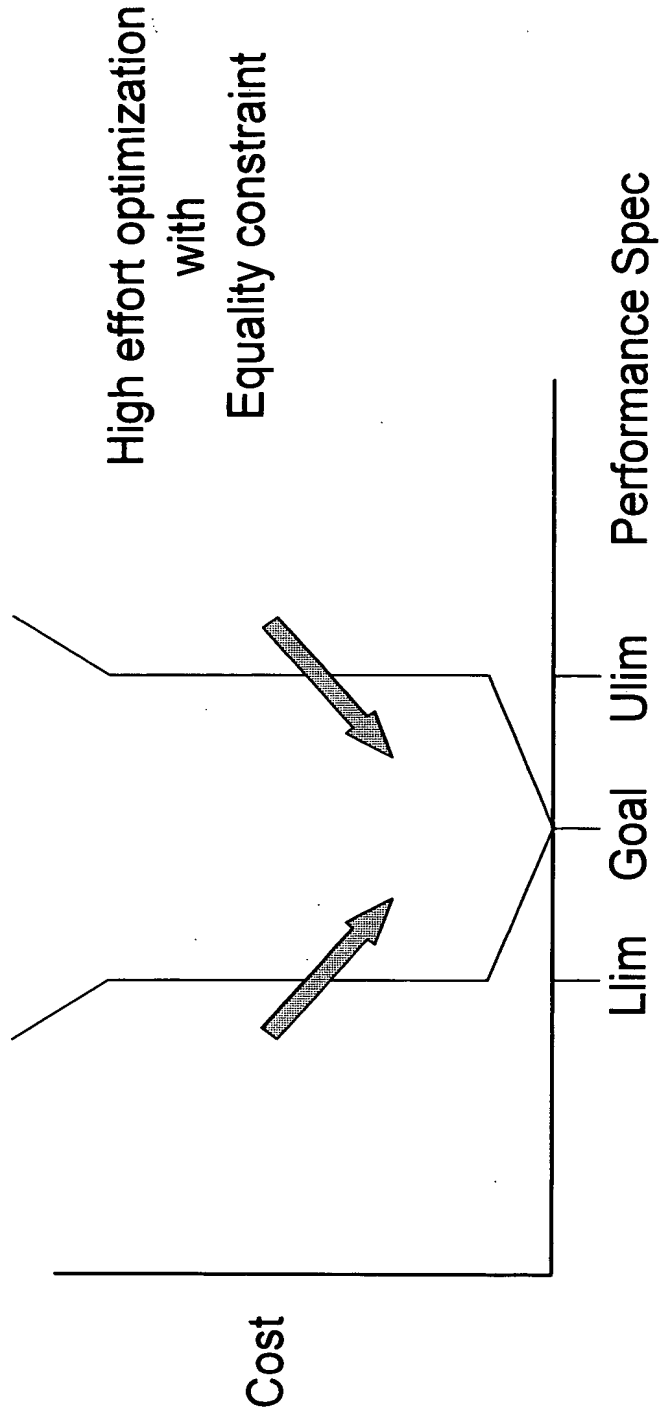


FIG. - 4A

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Cost Function

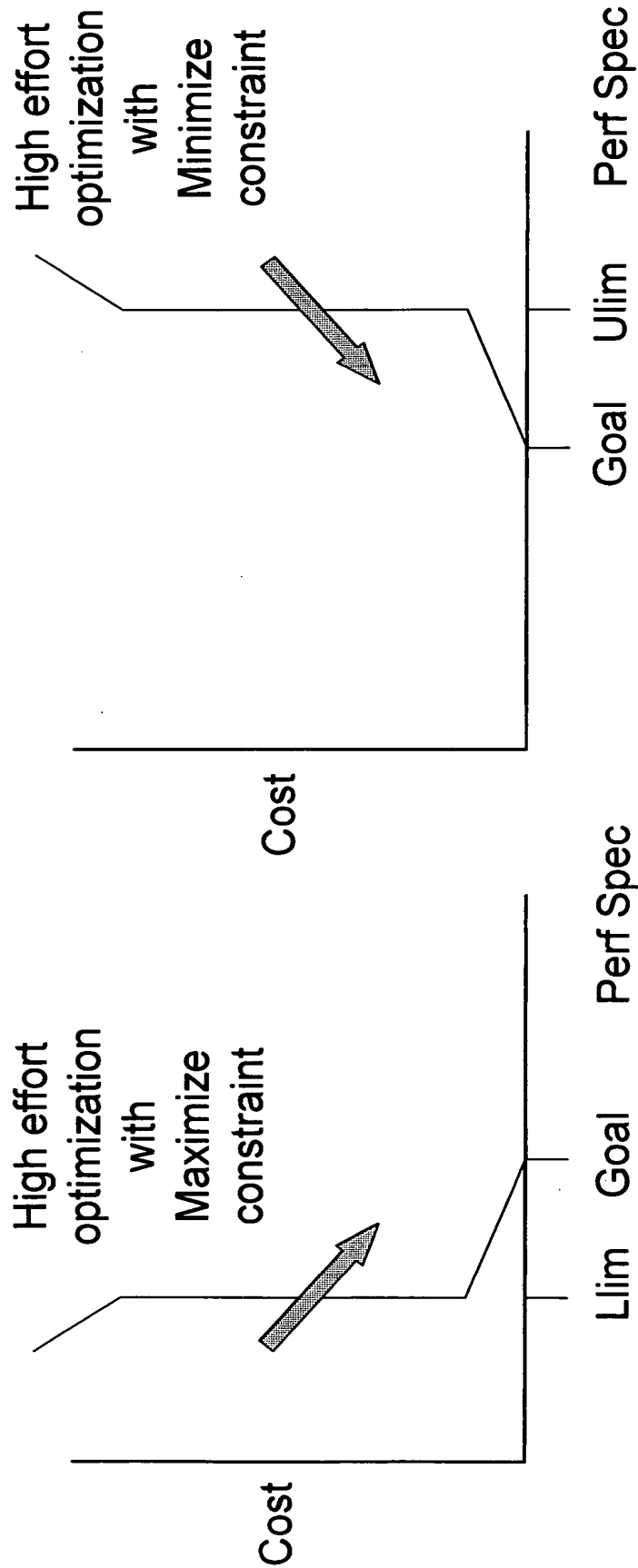


FIG. - 4B

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Cost Function

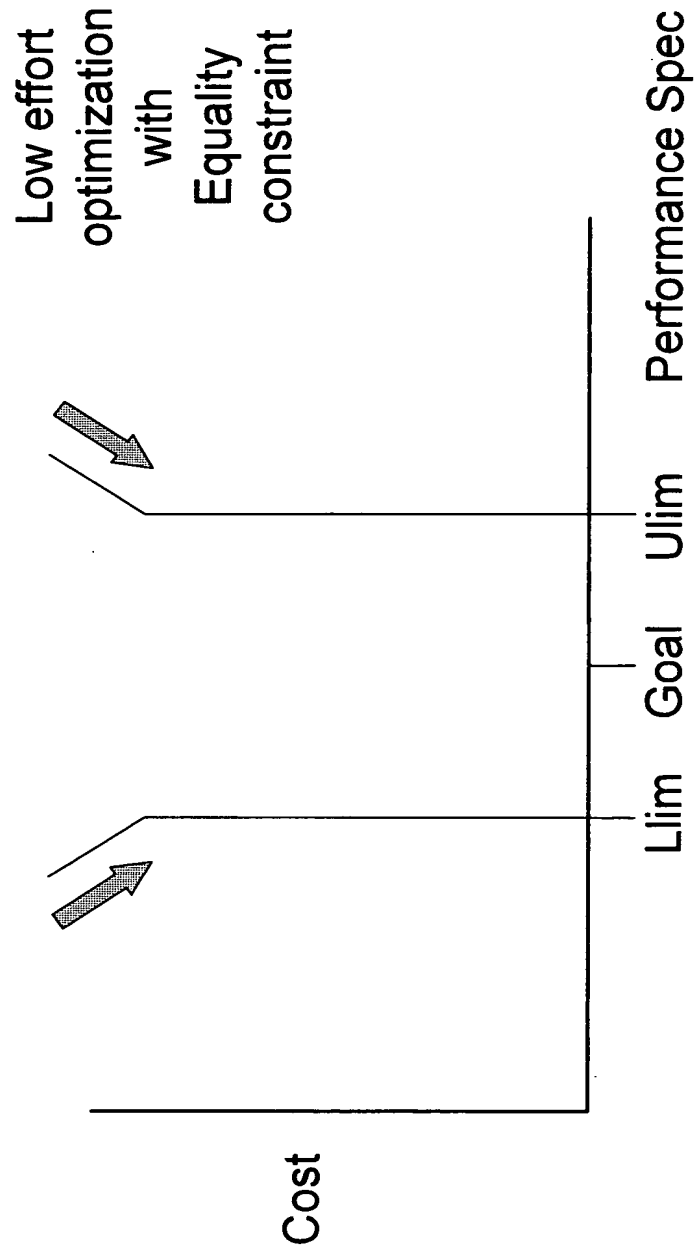


FIG. - 4C

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Cost Function

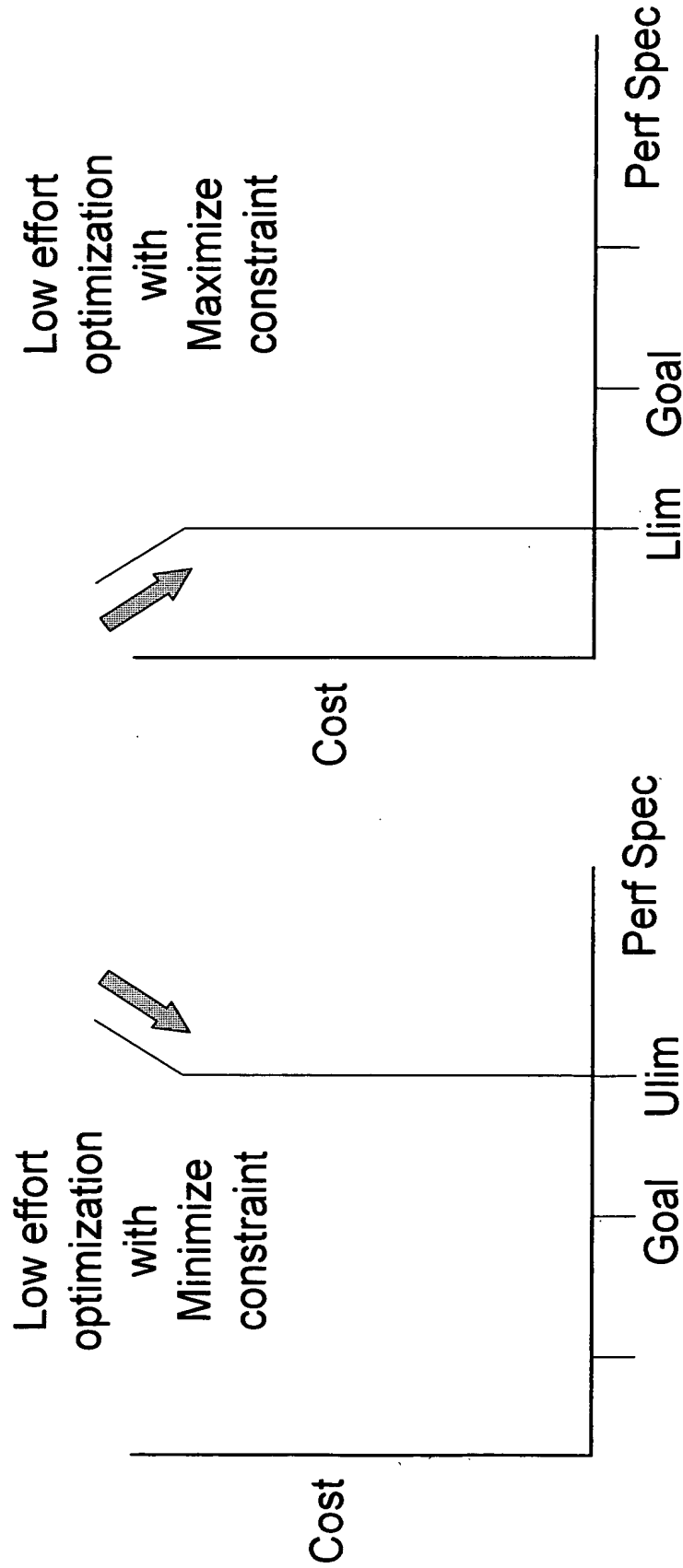


FIG. - 4D

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Example: Synthesis Plan for a VCO

Step One

- Size bias transistor for power specification
- 1st step - budget power according to user specification

$$P_{\text{tot}} = P_{\text{bias}} + 8 * P_{\text{delay}}$$
- NMOS transistor must remain in triode region with $V_{\text{ds}} = V_{\text{diode}}$
- Minimize W_{bias} & L_{bias} to meet spec

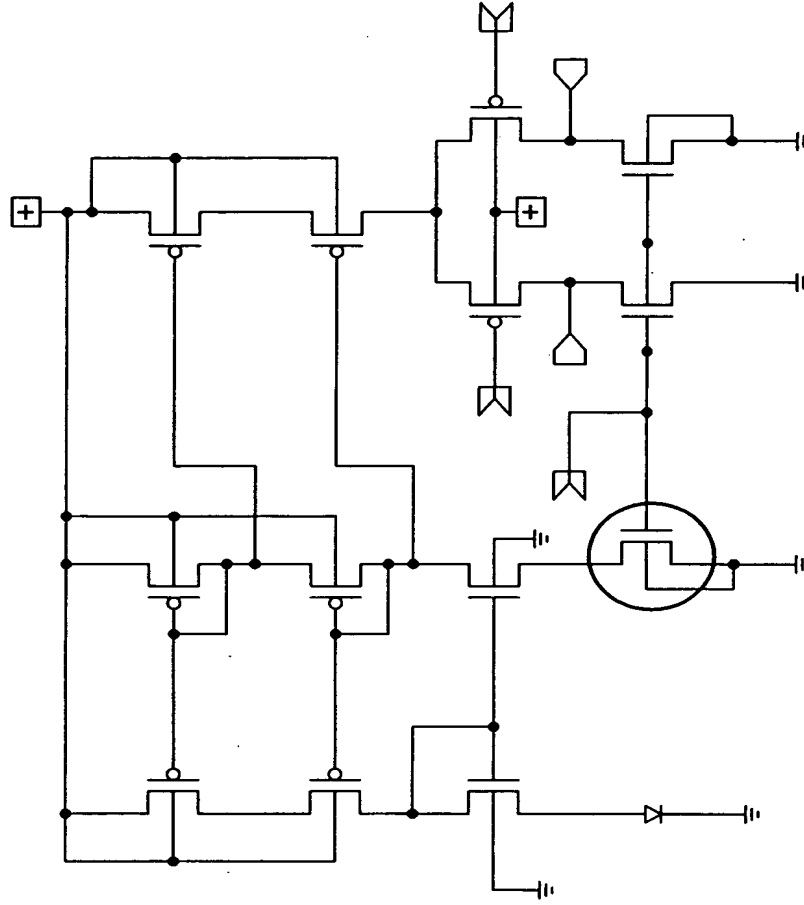


FIG. - 5

Example: Synthesis Plan for a VCO

Step Two

- Mirror NMOS transistors from bias cell
- Size delay cell transistors for frequency spec
- Use behavioral model of F_0 vs. W_{diff} , L_{diff}
- Minimize diff. pair for input load in ring oscillator
- Set L_{diff} to L_{min}
- Optimize W_{diff}

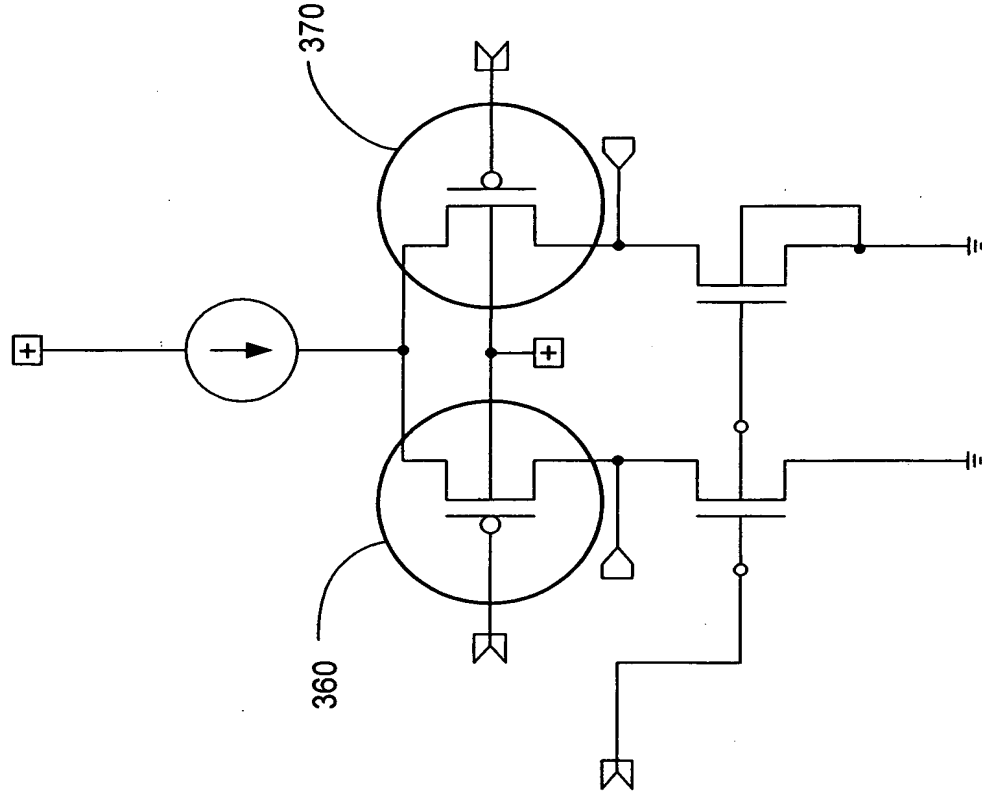


FIG. - 6

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Example: Synthesis Plan for a VCO

Step One

- Size bias transistor for power specification
- Measure current with condition $V_{ds} = V_{diode}$
- Minimize W_{bias} & L_{bias} to meet spec
- Analysis Setup:
 - simulate nbias_ivdc.v
 - test harness for bias current sizing
 - analysis = bias.tst
 - measurement experiment for current

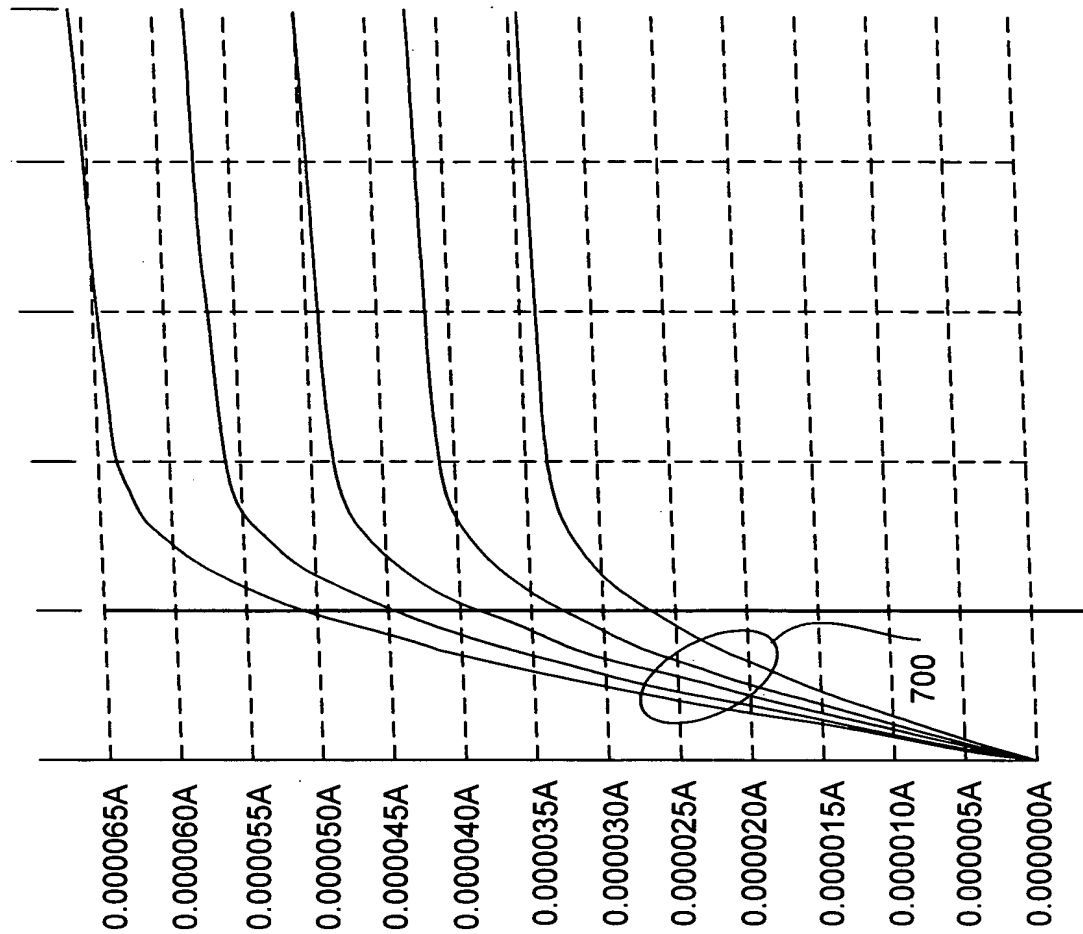


FIG. - 7

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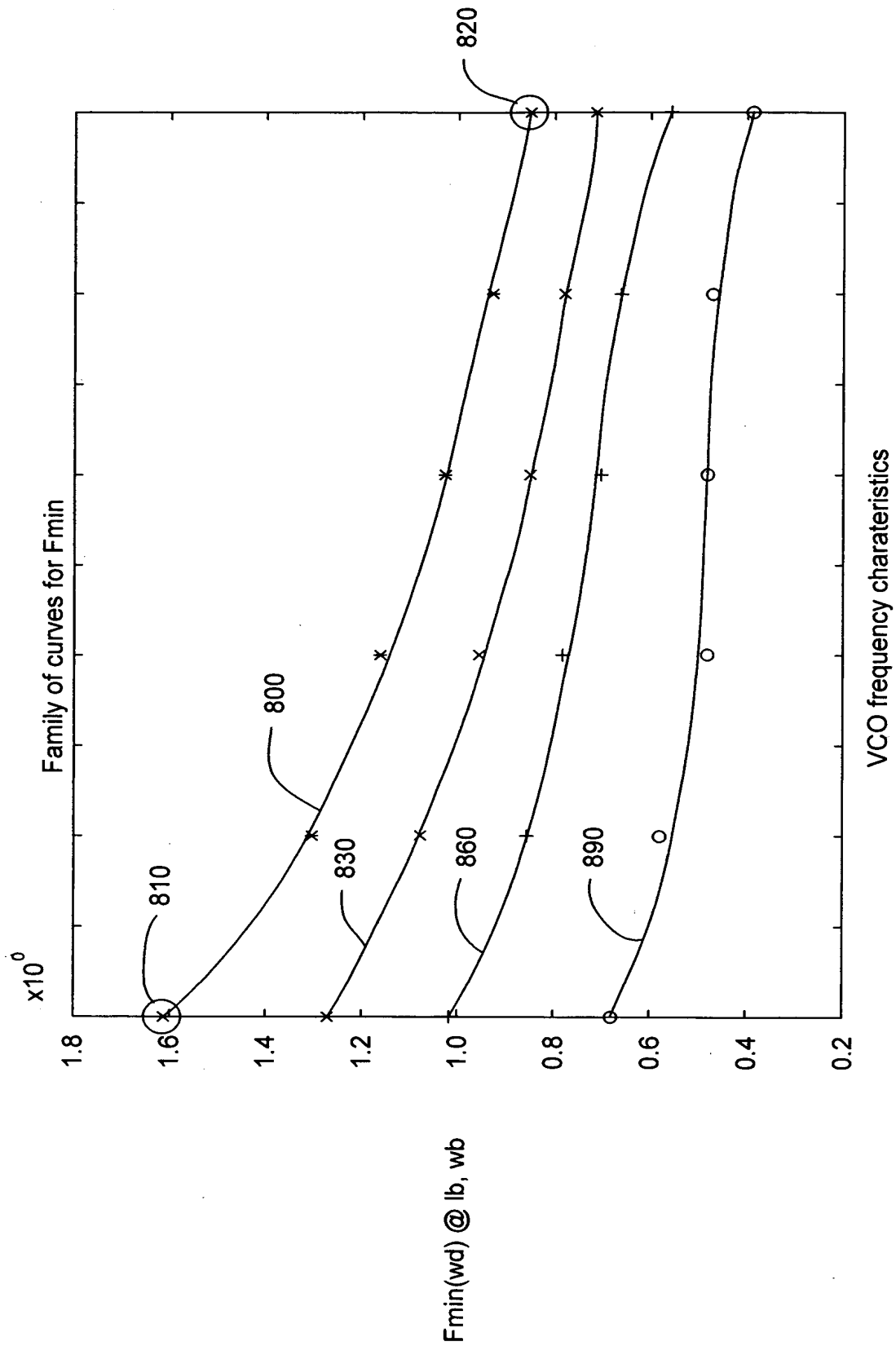
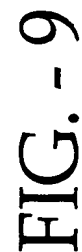


FIG. - 8

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Example: Synthesis Plan for a VCO *Step One*

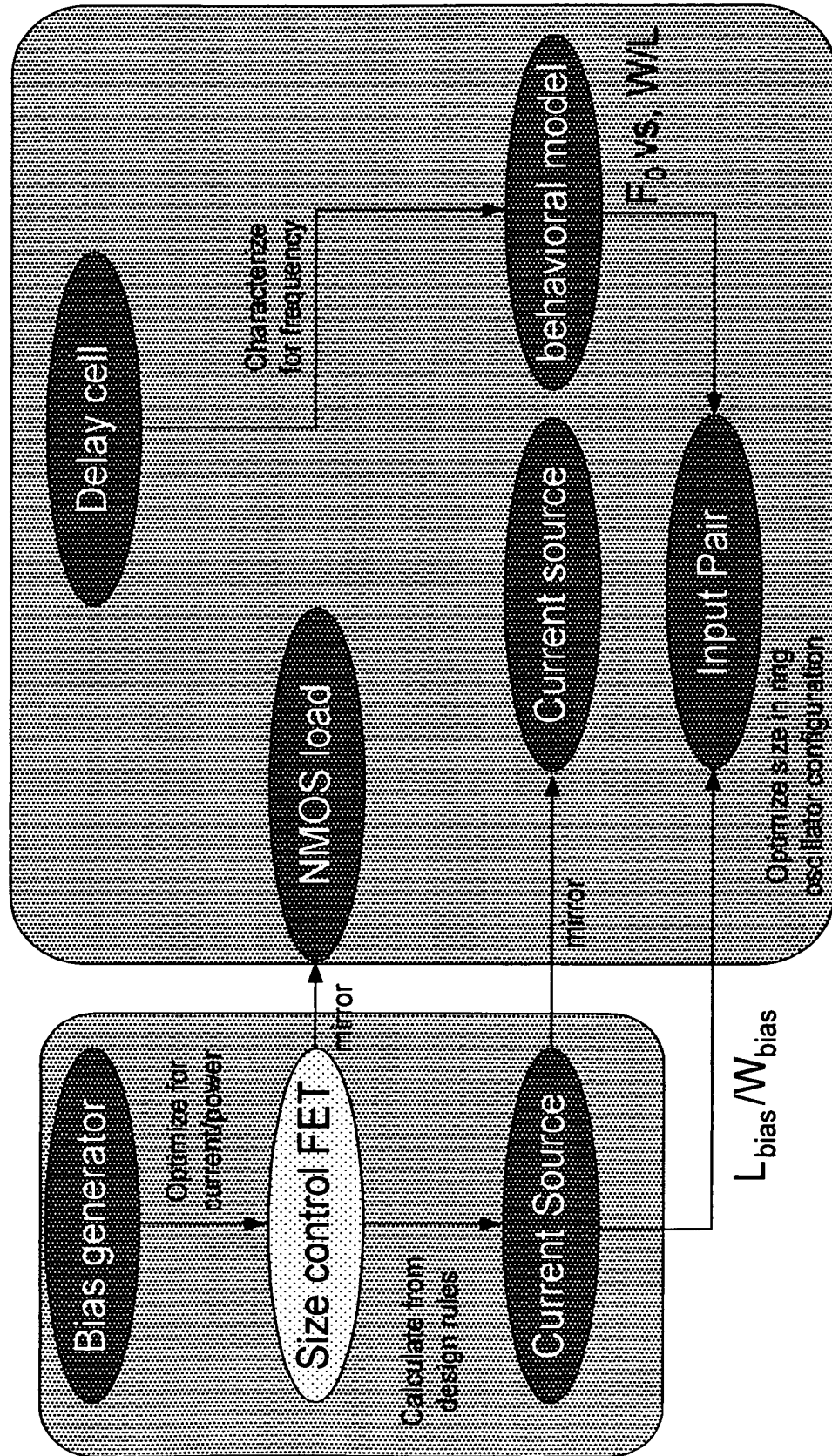


FIG. - 10

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Example: Synthesis Plan for a VCO

Step Two

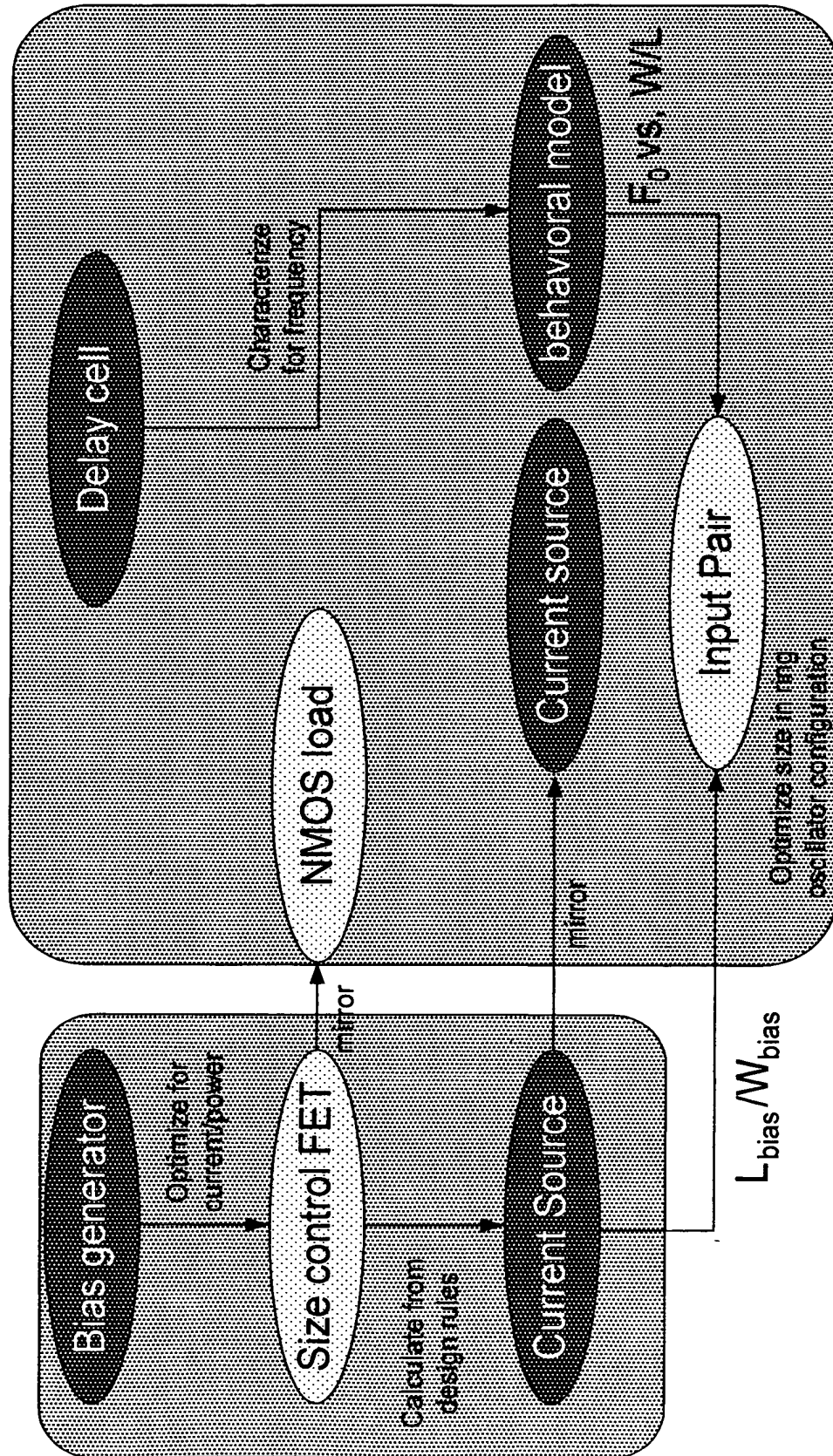


FIG. - 11

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Example: Synthesis Plan for a VCO

Finish Steps

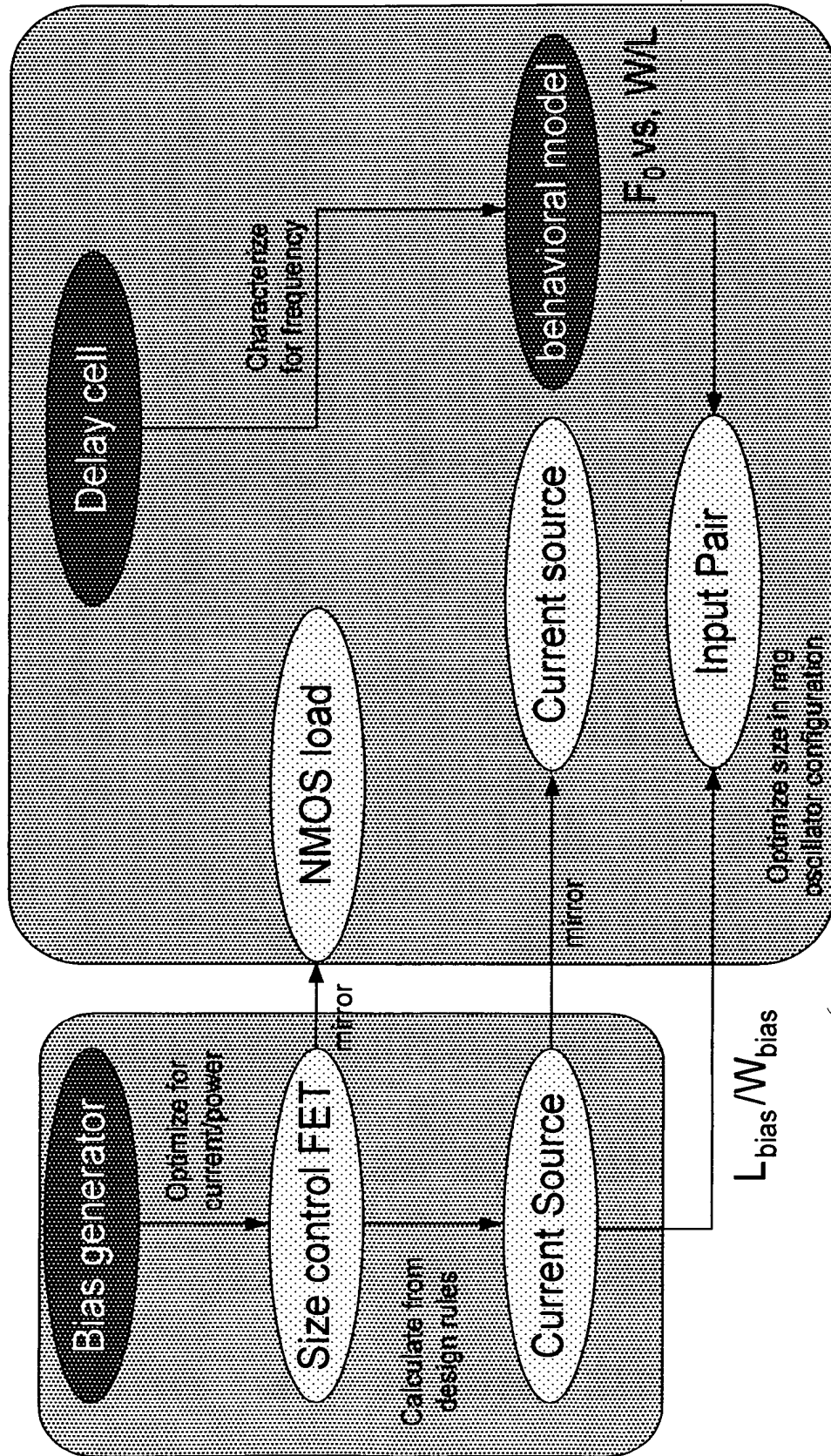


FIG. - 12

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Synthesis Plan for a VCO

Finish Steps

- Size noncritical MOSFETs in current sources
 - doesn't require optimization
- Synthesize level translator
- Verify complete design
- Could add other performance specifications
 - gain
 - F_{\min}
 - F_{\max}

FIG. - 13